What is claimed is:

1. A solid-state image sensor having a readout architecture that incorporates charge multipliers, said image sensor including:

a first CCD register adjacent to at least a second CCD register and coupled to the said first register through a charge overflow barrier.

2. The image sensor according to claim 1 wherein the second adjacent CCD register collects overflow charge and transports it to at least one detection node located in each register, and

each charge conversion node having charge conversion sensitivity that may be different for each node.

3. The image sensor according to claim 2, wherein signals from adjacent register detection nodes are processed and combined according to a predetermined mathematical formula.

4. A solid-state image sensor having a readout architecture that incorporates charge multipliers, said image sensor including:

a CCD register that incorporates at least one charge-multiplication device element in at least one stage and said at least one stage has a progressively wider width.

5. The image sensor according to claim 4, wherein the width of the CCD register-stages and the number of charge-multiplication elements in at least some of its stages varies according to a predetermined formula.

6. The image sensor according to claim 5, wherein the predetermined formula has an exponential dependency on the number of CCD stages that include charge multiplication devices.

7. The image sensor according to claim 4, wherein the CCD register includes a clearing gate and a clearing drain to remove unwanted charge.

8. The image sensor according to claim 4, wherein the CCD register has a charge overflow barrier and a charge overflow drain incorporated in at least one of its stages to prevent charge blooming.

9. A solid-state image sensor having a readout architecture, said readout architecture incorporating:

charge multipliers;

CCD registers; and

a charge overflow device in at least one of its registers.

10. The image sensor according to claim 4, wherein the sensor is oriented in a one crystallographic direction on the semiconductor substrate, and wherein the charge flows in said one direction through a high electrical field to minimize charge multiplication noise.

12. The image sensor according to claim 4, wherein the sensor is oriented in a one crystallographic direction on the semiconductor substrate wherein charge flows in that one direction through a high electrical field to minimize charge multiplication pulse amplitude.